Please replace the paragraph beginning at page 6, line 2 with the following new paragraph:

What is needed is a method of integrating a system with a microcontroller and integrated circuits (ICs) on a single chip to effectuate a single-chip system, including analog functionality, and/or a system so integrated with a microcontroller and/or other IC. What is also needed is a single-chip system which has sufficient flexibility to function in a very wide range of multiple applications, including applications wherein integrated analog functionalities are required. Further, what is needed is a method of programming and dynamically reconfiguring a single-chip system, and a single-chip system which is so programmable and dynamically reconfigurable. Further still, what is needed is a single-chip system which achieves the foregoing advantages and yet is relatively inexpensive and simple to configure, apply, use, and reconfigure.

Please replace the paragraph beginning at page 6, line 13 with the following new paragraph:

Embodiments of the present invention provide an integrated system with a microcontroller and integrated circuits (ICs) on a single chip to effectuate a single-chip system, including programmable analog and digital functionality and a microprocessor, and a method of configuring such an integrated system. The present invention also provides a single-chip system which has sufficient flexibility to function in a very wide range of multiple applications, including applications wherein integrated analog functionalities are required. Further, the present invention provides a method of programming and dynamically reconfiguring a single-chip system, and a single-chip system which is so programmable and dynamically reconfigurable. Further still, the present invention provides a single-chip system which achieves the foregoing advantages and yet is relatively inexpensive and simple to configure, apply, use, and reconfigure.

Please replace the paragraph beginning at page 7, line 13 with the following new paragraph:

In one embodiment, the present invention provides a method of integrating a system with a microcontroller/ IC on a single chip to effectuate a single-chip system, including programmable analog functionality. Another embodiment provides a system so integrated with a microcontroller/ IC. In one embodiment, the present invention also provides a single-chip system which has sufficient flexibility to function in a very wide range of multiple applications, including applications wherein integrated analog functionalities are required. In the present embodiment, the single-chip system is capable of executing a wide range of applications requiring programmable mixed (analog and digital) signals. In the present embodiments, both digital and analog functionalities are effectuated in block components integrated with a microcontroller/ IC on a single chip. These block components are complete functional units, each with a very large number of operations programmed within them.

Please replace the paragraph beginning at page 7, line 26 with the following new paragraph:

In one embodiment, the present invention further provides a method of programming and dynamically reconfiguring a single-chip system, and a single-chip system which is so programmable and dynamically reconfigurable. The programming is effectuated, in one embodiment, by firmware executing a series of instructions run by a microprocessor component of the microcontroller/ IC. In one embodiment, a new microcontroller/ IC programming paradigm is effectuated, wherein a user of the single-chip system loads a configuration into the functional blocks and/or programmable interconnects electrically coupling the functional blocks with each other, with other microcontroller components, and with the outside world.

Please replace the paragraph beginning at page 8, line 9 with the following new paragraph:

In one embodiment, the programmable interconnects configure, not only the functional blocks, but also the way in which the functional blocks intercommunicate. In one embodiment,

actual connection pins of the device can be configured to communicate with different internal resources, allow intercommunication via different methods and/or modalities, and actual reconfiguration of the internal structure of the device. In one embodiment, the reconfigurability features effectuate dynamic reconfiguring and programming, with no need to take the single-chip system out of service. The single-chip system can be dynamically reconfigured "on the fly," easily and in very little time. Advantageously, these features effectuate the ability to program microcontroller/ IC sequences and simultaneously program unique hardware functions that are expressible via the newly configured single-chip system.

Please replace the paragraph beginning at page 8, line 21 with the following new paragraph:

In one embodiment, the present invention provides a single-chip system which achieves the foregoing advantages and yet is relatively inexpensive and simple to configure, apply, use, and reconfigure. The inherent great flexibility and widespread applicability of microcontroller systems of the present embodiments obviates searching, shopping, and research for the "right" microcontroller and mix of functionalities and/or design and manufacture of custom microcontroller and mix of system functionalities. Real savings in effort, time, and cost are effectuated by embodiments of the present invention.

Please replace the paragraph beginning at page 16, line 18, with the following new paragraph:

With reference to Figure 1B, an exemplary integrated circuit (or microcontroller) 10 upon which embodiments of the present invention may be implemented is shown in greater detail. It is seen that system blocks 25 are constituted by at least three (3) distinct functionalities. These functionalities include analog system blocks 20, digital system blocks 100, and programmable interconnects 1000. Further, it is seen that the digital system blocks 100 and the analog system blocks 20 are coupled to the programmable interconnect 1000 by intra-block routing channels 1002.

The programmable interconnect 1000 is connected via an internal input/output (I/O) bus 1001 to pin by pin configurable I/O transceivers 18, which effectuate communicative coupling between system 10 and external modalities. The total pin count of pin by pin configurable I/O transceivers 18 may vary from one application to another, depending on the system device under consideration. A system timing block 19 is also coupled to programmable interconnect 1000.

Please replace the paragraph beginning at page 17, line 6 with the following new paragraph:

System timing block 19 includes system timing information used, among other things, for synchronizing and otherwise effectuating interfacing between system functionalities. System timing block 19, like system blocks 25, is programmable. Advantageously, this allows system timing block 19 to generate a myriad of different time bases, as required for any particular application the system is being configured to effectuate. These time bases may be fed into analog system blocks 20 and digital system blocks 100, for use therein, via programmable interconnect 1000. Examples of analog functions requiring such time bases, executed by analog system blocks 20 include conversions, modulations, and the like. One striking example of a digital function requiring such time bases, executed by digital system blocks 100 is their universal asynchronous receiver transmitter (UART) functionality.

Please replace the paragraph beginning at page 17, line 18 with the following new paragraph:

Referring to Figure 1C, system block 25 is depicted in greater detail. System block 25 is constituted, in one embodiment, by a distinct analog functional block 20, a distinct digital functional block 100, and a programmable interconnect 1000. Analog block 20 is seen to be constituted, in the present embodiment, by a matrix interconnecting internally N analog sub-blocks Al through AN. The number N may be any number of analog sub-blocks required for a particular application. Likewise, digital block 100 is seen to be constituted, in the present embodiment, by a matrix

C8

interconnecting internally M digital sub-blocks Dl through DM. The number M may be any number of digital sub-blocks required for a particular application.

Please replace the paragraph beginning at page 18, line 24 with the following new paragraph:

C9

A hierarchy of programmable interconnectivity is effectuated within system 10. Pin by pin configurable I/O transceivers 18 and input and output global mapping units 211 and 212, respectively, on programmable interconnect 1000, effectuate configurable interconnectivity between the system 10 and the "outside world," as well as the microcontroller SRAM, ROM, and CPU components 12, 16, and 14, respectively (Fig.'s 1A, 1B). These microcontroller components are communicated with via the system bus 11, and addressed via the programmable interconnect 1000 by the functional unit 25. Further, several sub-blocks within the analog and digital system blocks 20 and 100, respectively, are assigned addresses that are mapped onto system bus 11. Thus, the master computer system, e.g., the microcontroller, can re-write the blocks as memory functions, e.g., in SRAM 12.

Please replace the paragraph beginning at page 20, line 17 with the following new paragraph:

C10

Typically, configuration is static, and all blocks can be loaded with all of the requisite configuration register data in one operation. To change a particular subset of blocks from one configuration to another, another instruction is transferred from flash ROM 16 to the appropriate blocks. This is effectuated by a hardware subsystem 14S within the microcontroller CPU 14 that directly reads from flash ROM 16, over the internal address/system data bus 11, to the appropriate locale within system block 25. Advantageously, this informational sequencing is quite rapid, conserving time and computational resources. This hardware 14S may be thought of as a morph transmogrifier, loading new state tables to system block 25 functional units designated for a new functionality.

Please replace the paragraph beginning at page 21, line 10 with the following new paragraph:

One possible functionality, which may be an application of a system incorporating features of the present embodiment, is analog to digital (A/D) conversion. In performing A/D conversion, it is necessary to get signals entering on certain of the pins constituting parts of pin by pin configurable I/O transceivers 18 into the system block in the process. Owing to uncertainty in which block a user configuring the system 10 for A/D conversion will choose for performing the A/D conversion function, as well as uncertainty as to which pins the user will select for routing relevant signals, a mechanism is necessitated to achieve the requisite routing from the pin to the actual functional block inside the system; and vice versa, because a corresponding waveform will be generated in the functional block, which must be brought back out for use. Importantly, keeping in mind one advantageous feature of the present embodiment, that the design of embodiments of the present invention is not to dictate their applicability, but rather to effectuate implementation of the largest possible spectrum of applicability, the configurability of pin by pin configurable I/O transceivers 18, programmable interconnect 1000, and system blocks 25 may be crucial.

C11

Please replace the paragraph beginning at page 23, line 24 with the following new paragraph:

The following co-pending US application is hereby incorporated by reference, serial number 09/909,047, by Monte Mar, entitled "A Programmable Analog System Architecture," filed July 18, 2001, and which is assigned to the assignee of the present invention.

C12

Please replace the paragraph beginning at page 24, line 11 with the following new paragraph:

The analog system architecture can be generally referred to as a programmable analog "system-on-a-chip" block. Such programmable blocks can be used in those applications that typically require multiple chips that may be fabricated using different technologies. Implementation

C13

C13 in embedded applications, including audio, wireless, handheld, data communications, Internet control, and industrial and consumer systems, is contemplated.

Please replace the paragraph beginning at page 43, line 2 with the following new paragraph:

C14 The programmable digital circuit blocks can be configured to be coupled in series or in parallel to handle more complex digital functions. For example, a 24-bit timer can be designed by coupling three 8-bit programmable digital circuit blocks that have been individually configured as 8-bit timers. Additionally, a first programmable digital circuit block that is configured as a CRC generator can feed a second programmable digital circuit block that is configured as a serial output communication port. A variety of mathematical functions such as addition, multiplication, exponential, logarithmic, arithmetic and floating point operations, and a plethora of other mathematical functions may be effectuated herein.

Please replace the paragraph beginning at page 60, line 24 with the following new paragraph:

C15 In the present exemplary circuit, a number of registers are configured to store programming data for the programmable digital circuit blocks. Some number of latches are configured to store programming data for the programmable analog circuit blocks.

Please replace the paragraph beginning at page 62, line 25 with the following new paragraph:

C16 The system is further constituted by an interconnecting mechanism, and the functionality further constituted by a first sub-functionality (e.g., analog system blocks 20; Fig. 1B, 1C) performing the analog functions and a second sub-functionality (e.g., digital system blocks 100; Fig. 1B, 1C) performing the digital functions. The interconnecting mechanism is configurable to interconnect the first sub-functionality and the second sub-functionality according to an input of a

C16

third type, e.g., an intrafunctionality (e.g., within system block 25; Fig. 1A, 1B, 1C) interconnection configuring program.

Please replace the paragraph beginning at page 63, line 15 with the following new paragraph:

C17

With reference to Figure 29, a process 2900 for configuring a system (e.g., system 10; Fig. 1B) is described. Beginning in step 2910, an analog and/or digital function is selected. This function may be effectuated in part by one or more functional units, e.g., functionalities, which may, in one embodiment, be analog and digital functionalities (e.g., analog and digital system blocks 20 and 100, respectively; Fig. 1B).

Please replace the paragraph beginning at page 65, line 26 with the following new paragraph:

C18

In summary, the present invention provides an integrated system with a microcontroller and integrated circuits (ICs) on a single chip to effectuate a single-chip system, including analog and digital functionality, and a method of configuring such an integrated system. The present invention also provides a single-chip system which has sufficient flexibility to function in a very wide range of multiple applications, including applications wherein integrated analog functionalities are required. Further, the present invention provides a method of programming and dynamically reconfiguring a single-chip system, and a single-chip system which is so programmable and dynamically reconfigurable. Further still, the present invention provides a single-chip system which achieves the foregoing advantages and yet is relatively inexpensive and simple to configure, apply, use, and reconfigure.

Please replace the paragraph beginning at page 67, line 9 with the following new paragraph:

C19

An embodiment of the present invention, a programmable microcontroller architecture, is thus described. While the present invention has been described in particular embodiments, it should